



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Reithinger, *et al.* Attorney Docket: 00P7685US
Filed: June 16, 2000 Examiner: Phat X. Cao
Serial No.: 09/596,129 Art Unit: 2814
For: Multiple Chip Semiconductor Arrangement having Electrical Components in
Separating Regions

Mail Stop: RCE
Commissioner for Patents
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Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.


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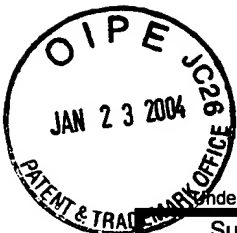
Respectfully submitted,

January 19, 2004

Date

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PTO/SB/08A (05-03)

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(use as many sheets as necessary)

Sheet

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of

1

Complete if Known

Application Number	09/596.129
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Filing Date	June 16, 2000
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First Named Inventor	Reithinger, et al.
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Art Unit	2814
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Examiner Name	Phat X Cao
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Attorney Docket Number	00P7685US
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	2	JP-01-220843	09-04-1989	NEC Corp.	English Abstract only	
	3	JP-63-234553	09-29-1988	NEC Corp.	English Abstract only	
	4	JP-04-171860	06-19-1992	Hitachi Ltd.	English Abstract only	
	5	JP-11-163062	06-18-1999	Toshiba Corp.	English Abstract only	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite ₁ No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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